Q.P. Code – 42144

First Semester B.Sc. Degree Examination, October/November 2019

(CBCS Scheme)

Electronics

Paper I - NETWORK ANALYSIS, ANALOG AND DIGITAL ELECTRONICS

Time : 3 Hours] *[Max. Marks : 90*

Instructions to Candidates : Answer any TEN questions from Part A, any FIVE questions from Part B, any FIVE questions from Part C and any FIVE questions from Part D.

PART – A

Answer any **TEN** questions : **(10 × 1 = 10)**

1. What is stiff voltage source?
2. What is a mesh in electrical network?
3. State Kirchhoff's current law.
4. Write the equivalent circuit of practical zener diode.
5. What is the PIV value of centre tapped full wave rectifier?
6. What is the value of knee voltage drop in Ge diode?
7. What is current gain in common emitter configuration?
8. Draw hybrid model of a transistor in CE configuration.
9. What is Q-point?
10. Write the excess-3 code for $475_{(10)}$.
11. How many bits are there in 4 kilo bytes?
12. Write the truth table of X-NOR gate.

PART – B

Answer any **FIVE** questions : **(5 × 8 = 40)**

13. (a) State and explain voltage divider theorem using three resistors in series.

(b) Obtain an expression for converting delta (π) network into star (T) network. **(4 + 4)**

14. (a) Write the steps to obtain Norton's equivalent circuit for T-resistive network.

(b) State superposition theorem and reciprocity theorem. **(4 + 4)**

15. (a) Explain the construction and working of Schottkey diode.

(b) Draw and explain v-I characteristics curve of a semiconductor junction diode. **(4 + 4)**

16. (a) Explain the working of half wave rectifiers. Draw waveforms.

(b) Derive expression for ripple factor and efficiency of half wave rectifier. **(4 + 4)**

17. (a) Draw output characteristics of a transistor in CE mode. Explain different regions.

(b) Explain fixed bias circuit and derive expression for stability factor. **(4 + 4)**

18. (a) With the circuit diagram explain the working of CE amplifier.

(b) Distinguish between class A, class B and class C amplifiers. **(4 + 4)**

19. (a) What are weighted and nonweighted codes? Give examples for each.

(b) Draw the circuit of two input diode OR gate and explain. Write its truthtable. **(4 + 4)**

20. (a) State and prove Demorgan's theorem.

(b) Show that :

(i) $A + \overline{A}B = A + B$

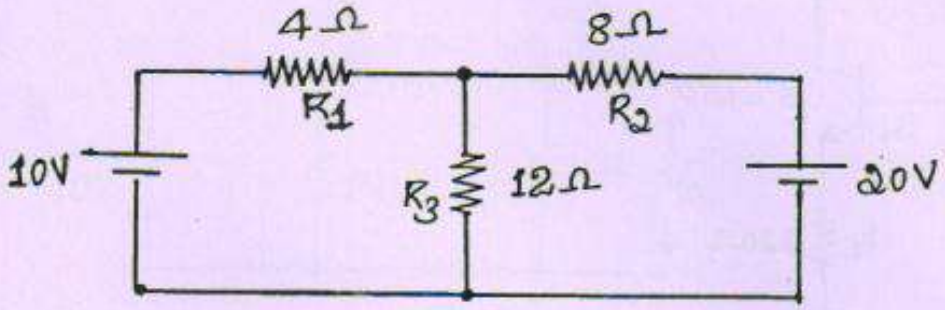
(ii) $A + AB + A\overline{B}C = 1$

(iii) $(A\overline{B}C + \overline{A}\overline{B})C = \overline{B}C$. **(4 + 4)**

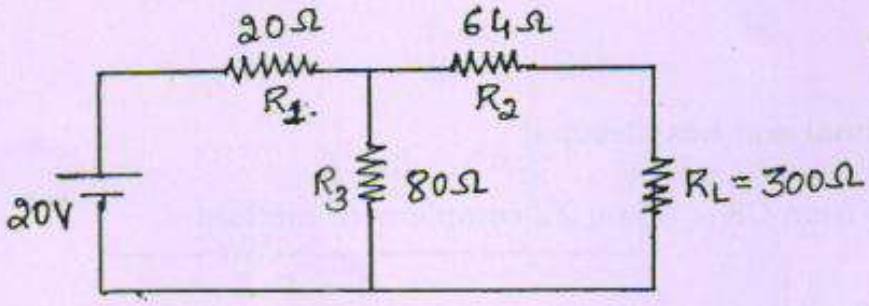
PART – C

Answer any **FIVE** questions : **(5 × 6 = 30)**

21. Find all branch currents using mesh current analysis. Also calculate potential difference across 12Ω resistor.



22. Determine the load current (I_L) in R_L using Thevenin's theorem.

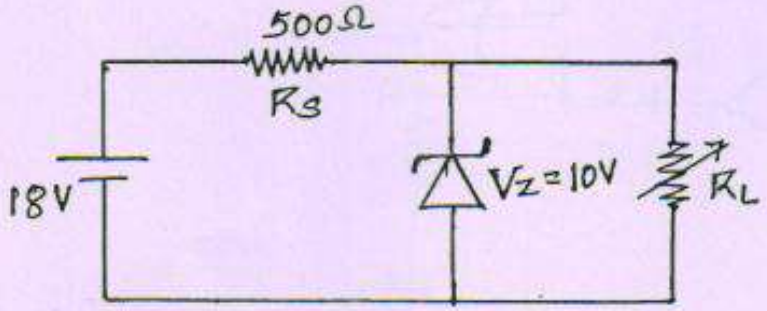


23. The transformer used in bridge rectifier circuit has the term ratio of 8 : 1 and the primary is connected to mains supply 240 V, 50 Hz. If the load resistance used in the circuit in 800Ω. Calculate

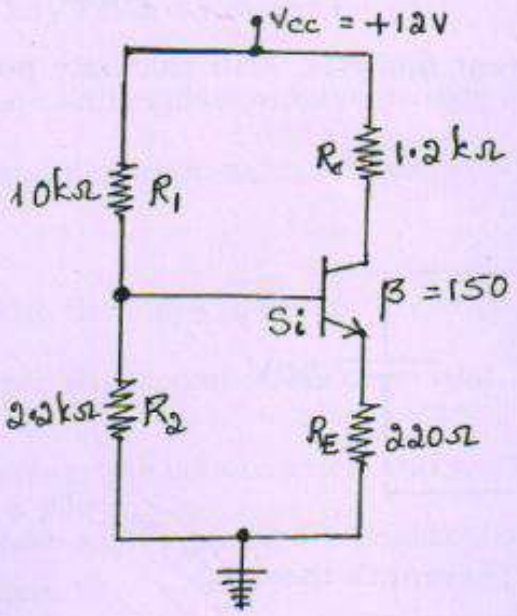
    (a) DC voltage and current

    (b) Ripple factor.

24. Find the range of load resistors in which the zener regulator shown will maintain 10 V across the load. $I_{z(min)}$ = 3 mA and $I_{z(max)}$ = 12 mA.



25. Locate Q point on the dc load line.



26. Convert :

(a) $376_{(8)}$ into decimal and hexadecimal

(b) Subtract $2B_{(16)}$ from $C8_{(16)}$ using 2's complement method. **(3 + 3)**

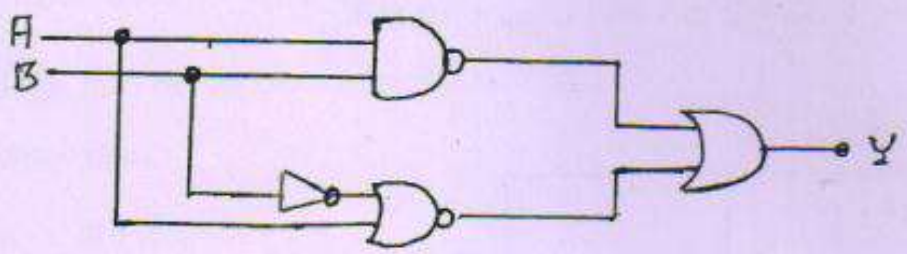
27. (a) Perform the following :

(i) $101101_{(2)} + 110011_{(2)}$

(ii) $110101 - 101110_{(2)}$

(iii) $EB_{(16)} + 81_{(16)}$.

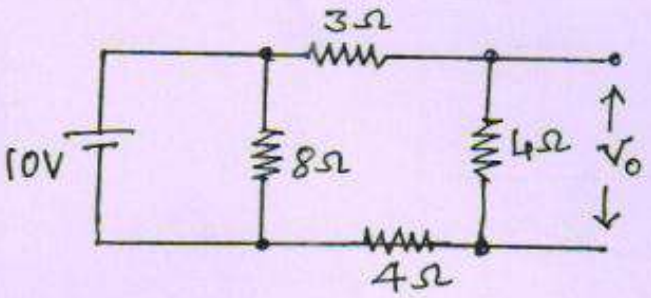
(b) Obtain the expression for the circuit shown below :



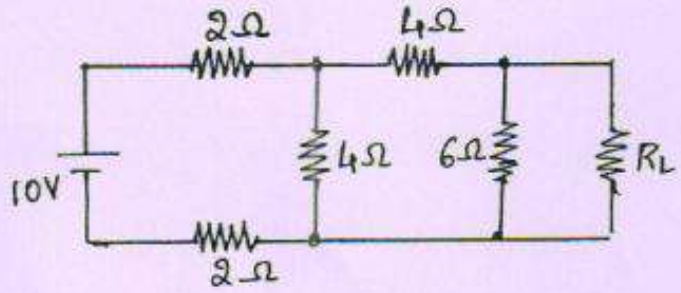
PART – D

Answer any **FIVE** questions : **(5 × 2 = 10)**

28. Find the output voltage V_0 when 3Ω resistor in (a) open (b) short.

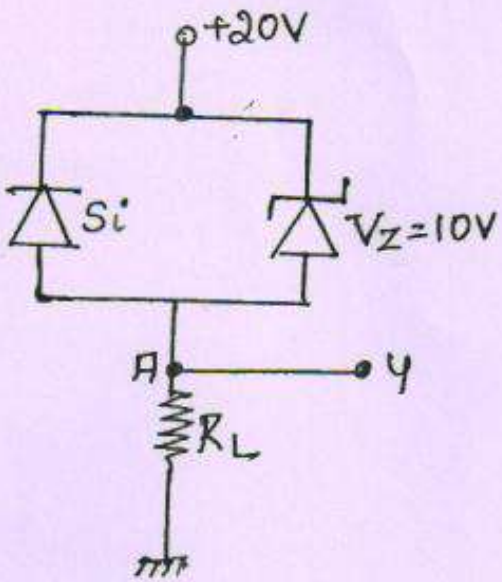


29. What should be the value of R_L so that maximum power is delivered?



30. (a) What is the voltage at point A?

(b) If Si diode is reversed what is the value of the voltage at A?



Q.P. Code – 42144

31. Can we use zener diodes in rectifier circuits? Justify?

32. Can you interchange emitter and collector in a transistor? Justify.

33. Write the ASCII code for B and 3.

34. Implement the following logic equation using basic gates.

$$Y = \overline{\bar{A}B + B\bar{C} + A\bar{B}C}$$